


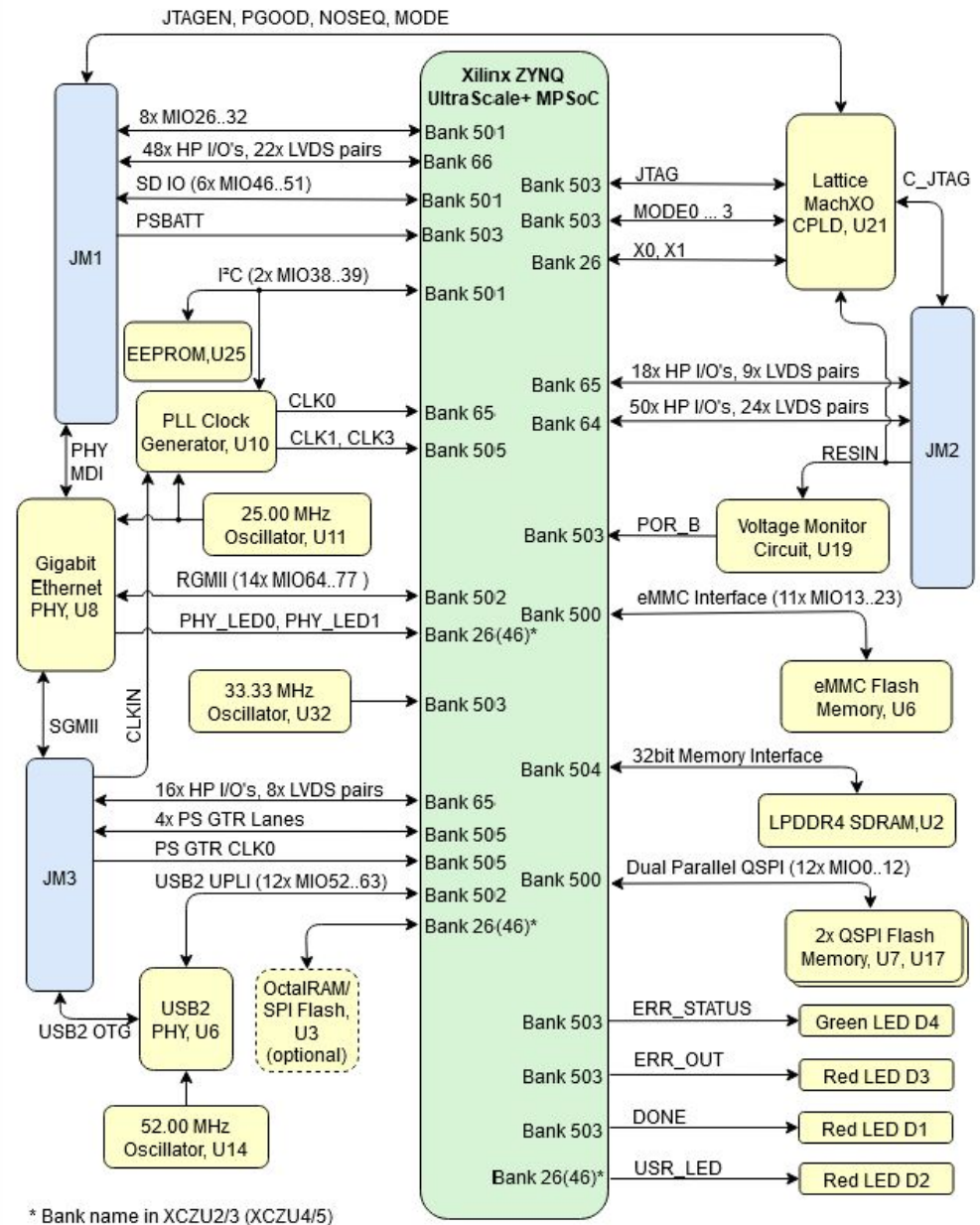
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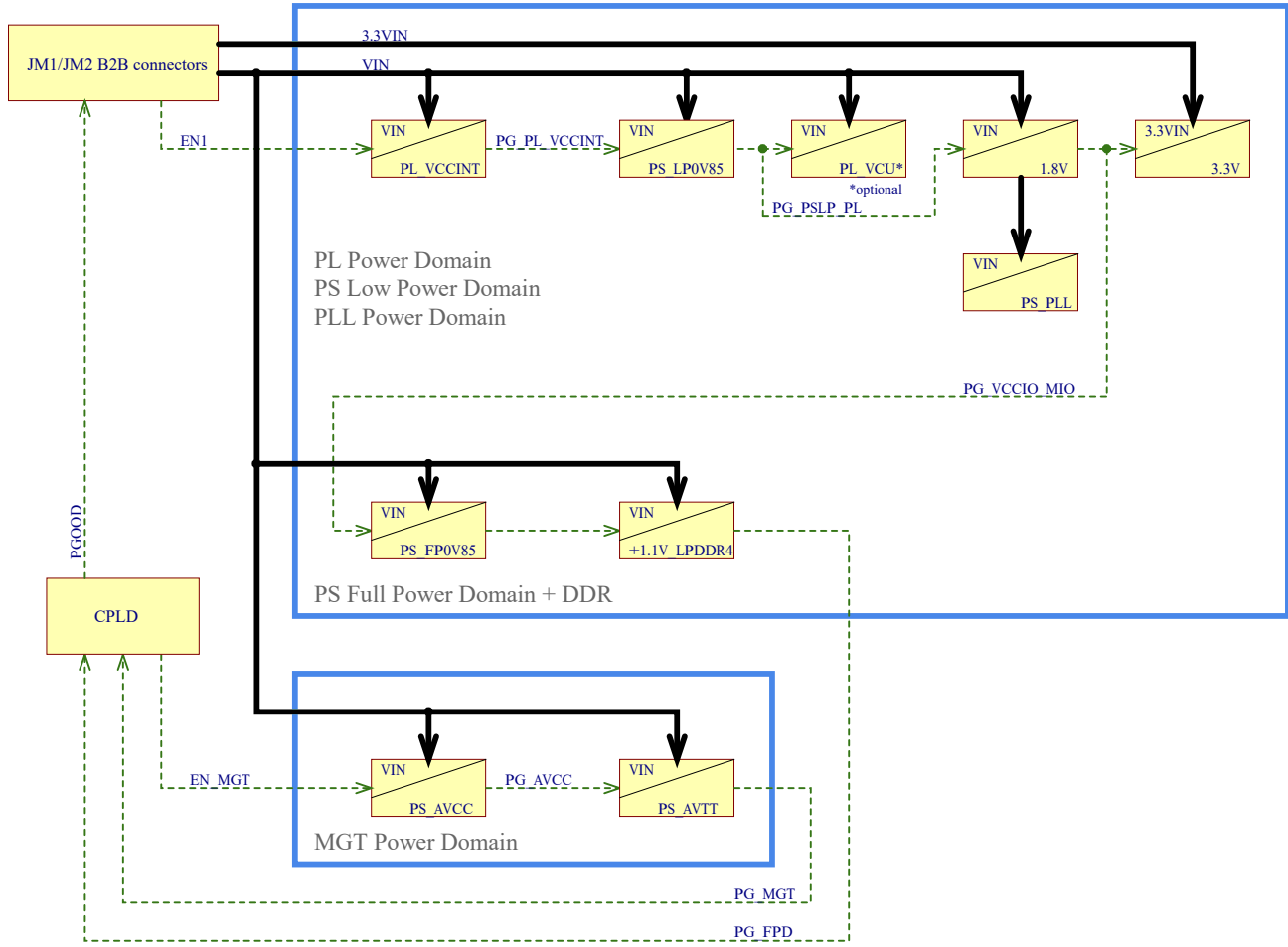
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	Title: TE0823 - Legal notices		
	A4	Number: TE0823 [No Variations]	Rev. 01
	Date: 2020-10-29	Copyright: Trenz Electronic GmbH / TT	Page 1 of 25
	Filename: Legal Notices Modules.SchDoc		

TE0823



	Title: TE0823 - System Overview		
	A4	Number: TE0823 [No Variations]	Rev. 01
	Date: 2020-10-29	Copyright: Trenz Electronic GmbH	Page 2 of 25
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			Title: TE0823 - Power Overview	
			A4	Number: TE0823 [No Variations]
Date: 2020-10-29		Copyright: Trenz Electronic GmbH		Page 3 of 25
Drawn by: VY		Filename: TE0823-Power-Overview.SchDoc		

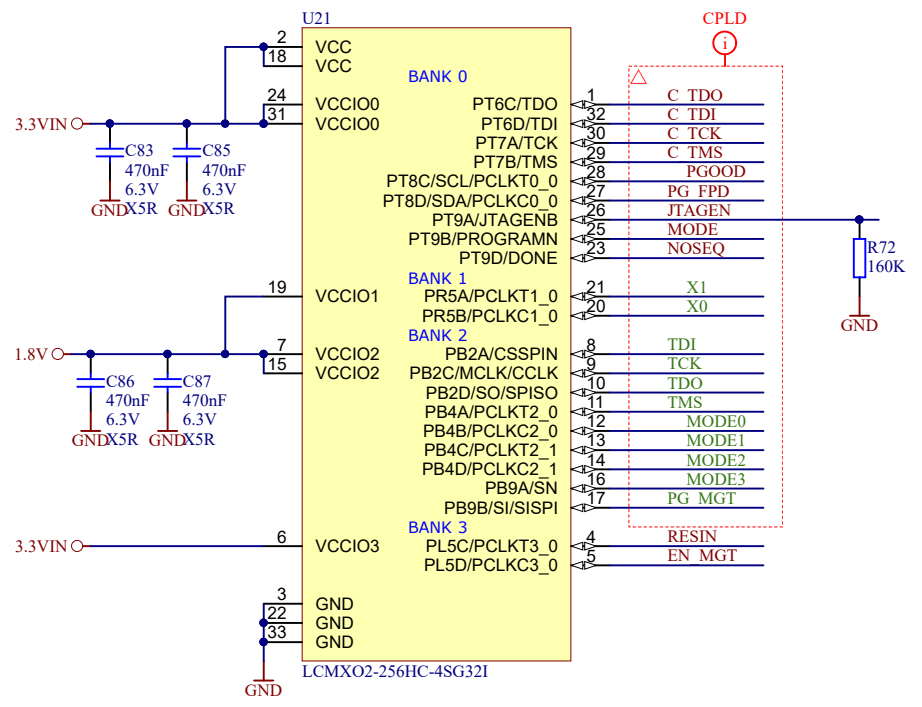
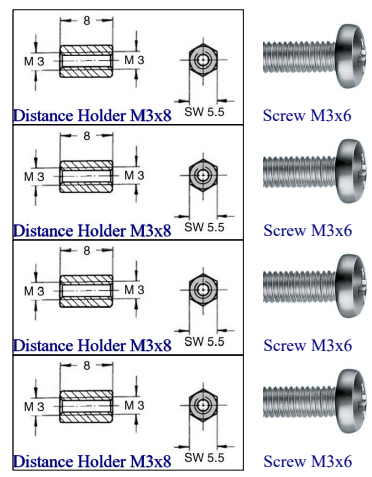
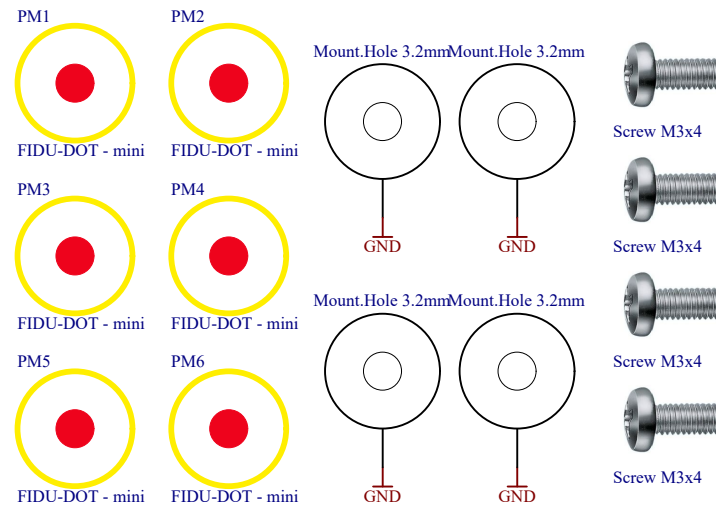
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U_ETH-PHY	ETH-PHY.SchDoc
U_B_HD	B_HD.SchDoc
U_B64	B64.SchDoc
U_B65	B65.SchDoc
U_B66	B66.SchDoc
U_CONFIG	CONFIG.SchDoc
U_B_MIO	B_MIO.SchDoc
U_B_PS_GT	B_PS_GT.SchDoc
U_CLK	CLK.SchDoc
U_Revision_Changes	Revision Changes.SchDoc
U_POV	TE0823-Power-Overview.SchDoc

U_B2B-Connectors	B2B-Connectors.SchDoc
U_eMMC	eMMC.SchDoc
U_PS_DDR	PS_DDR.SchDoc
U_ZU_POWER	ZU_POWER.SchDoc
U_ZU_PS_POWER	ZU_PS_POWER.SchDoc
U_LPDDR4	LPDDR4.SchDoc
U_POWER	POWER.SchDoc
U_POWER_1	POWER_1.SchDoc
U_HyperRAM	HyperRAM.SchDoc
U_Overview	TE0823-Overview.SchDoc
U_B2B-Connectors_2	B2B-Connectors_2.SchDoc
U_LN	Legal Notices Modules.SchDoc

I2C-Address	Component
0x50	24AA025E48T-I/OT
0x70	SI5338A-B-GMR
0x..	PS MIO



Serial
Serialnumber 6,3 x 6.3mm



Assembly variant	[No Variations]
Created by	
Modified by	
Modified at	
SVN Revision	8870 [Locally Modified]

Title: TE0823 - System controller		
A4	Number: TE0823 [No Variations]	Rev. 01
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Drawn by: VY	Filename: TE0823.SchDoc	

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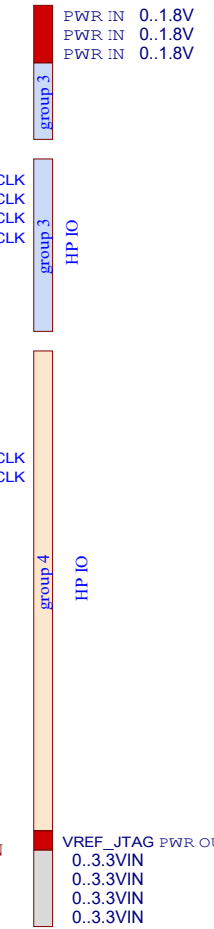
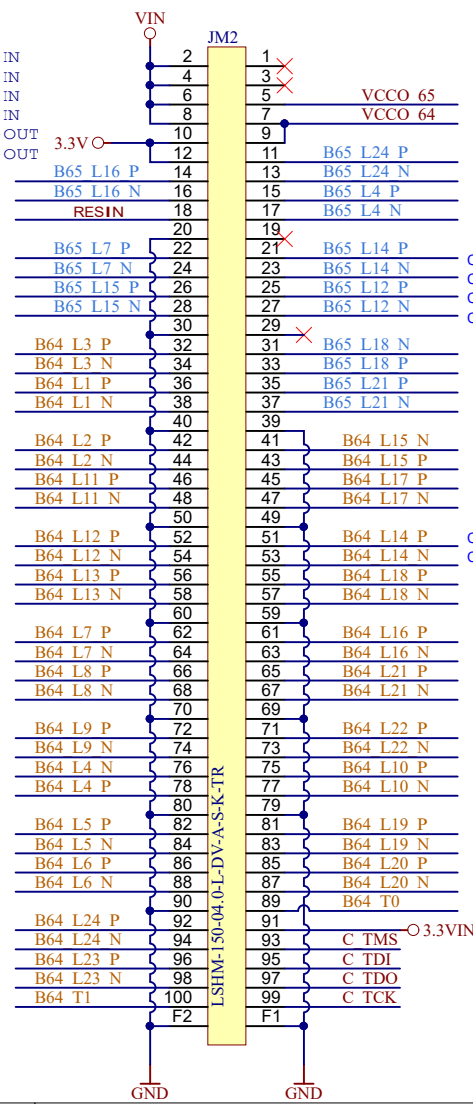
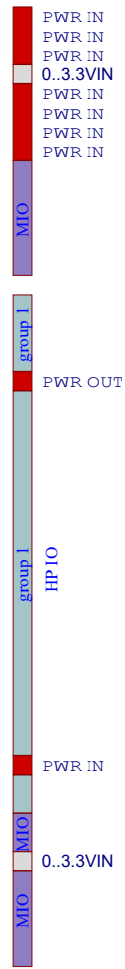
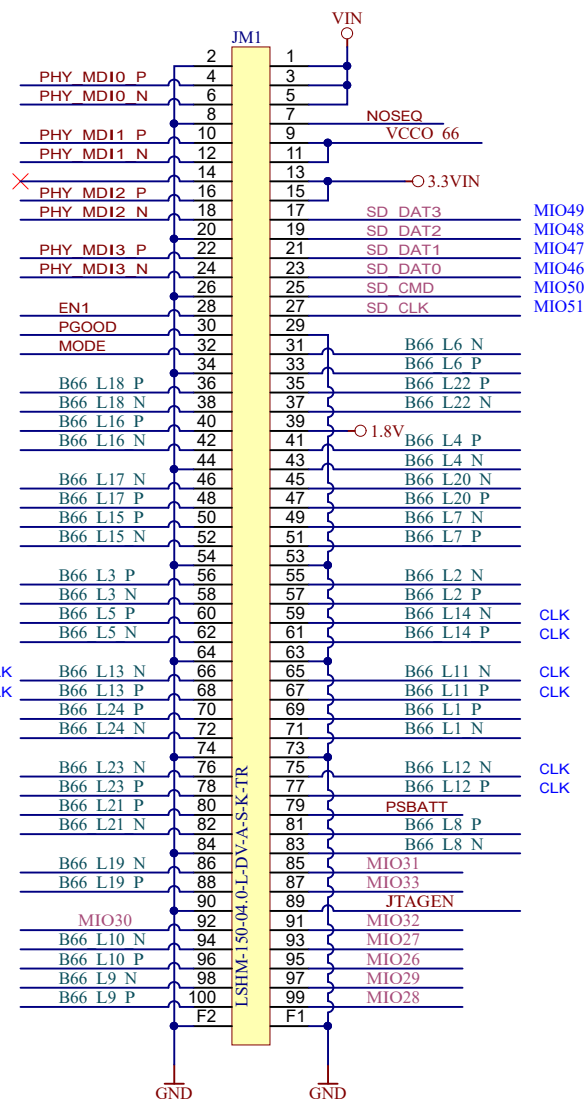
D

D

VCCO_64	0..1.8V
VCCO_65	0..1.8V
VCCO_66	0..1.8V
MIO	0..3.3V
group 1	0..VCCO_66
group 3	0..VCCO_65
group 4	0..VCCO_64

ETH MDI Copper
 B64(HP) 50 IO, 24 LVDS Pairs
 B65(HP) 18 IO, 9 LVDS Pairs
 B66(HP) 48 IO, 24 LVDS Pairs

0..3.3VIN (PU)



PU - On board pull-up resistor
 PD - On board pull-down resistor



Title: TE0823 - B2B Connectors		
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1

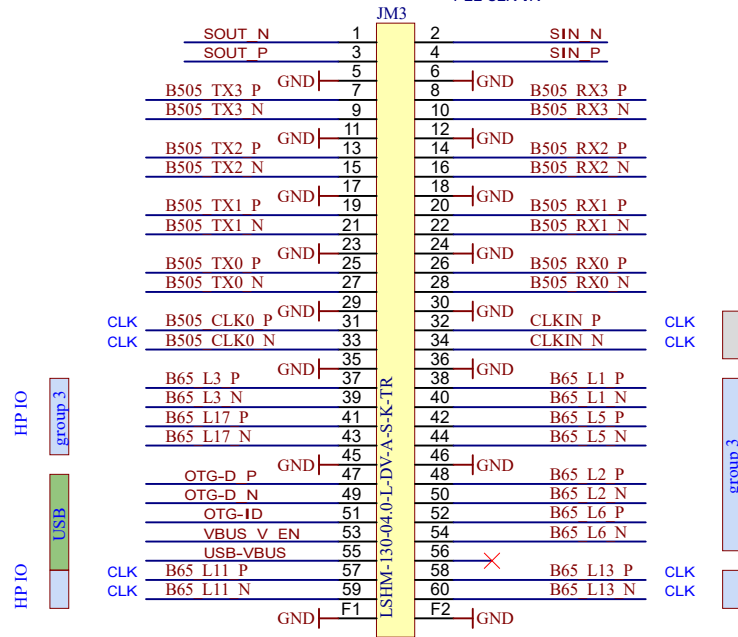
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B65(HP) 16 IO, 8 LVDS Pairs
 USB OTG
 ETH SGMII
 PS_GTR 4 Lanes
 PS_GTR CLK IN
 PLL CLK IN

group 3 0..VCCO_65



VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

	Title: TE0823 - B2B Connectors		
	A4	Number: TE0823 [No Variations]	Rev. 01
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	Drawn by: VY	Filename: B2B-Connectors_2.SchDoc	

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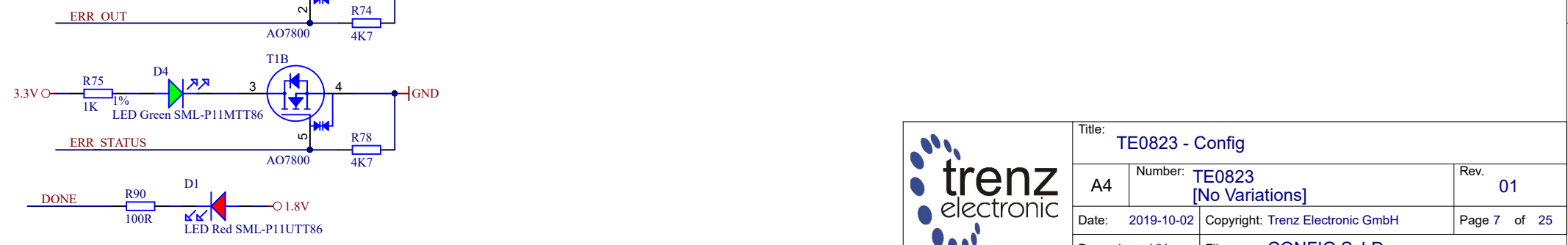
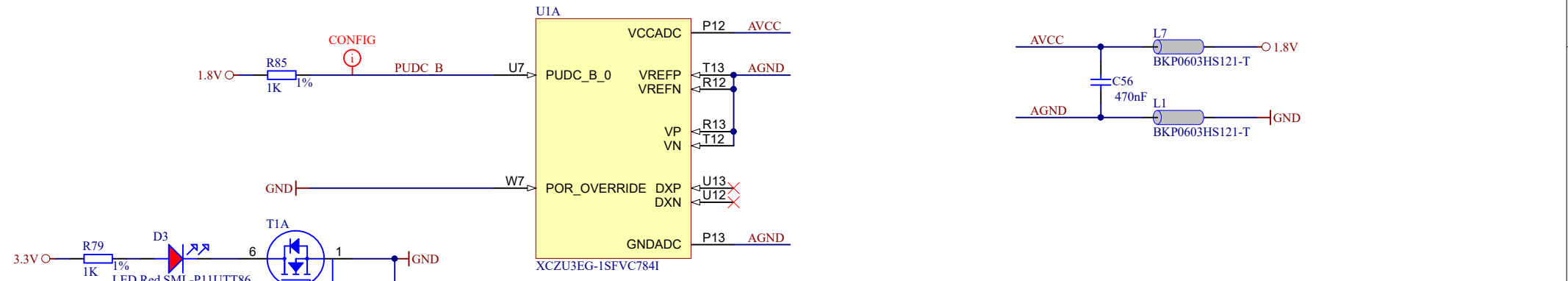
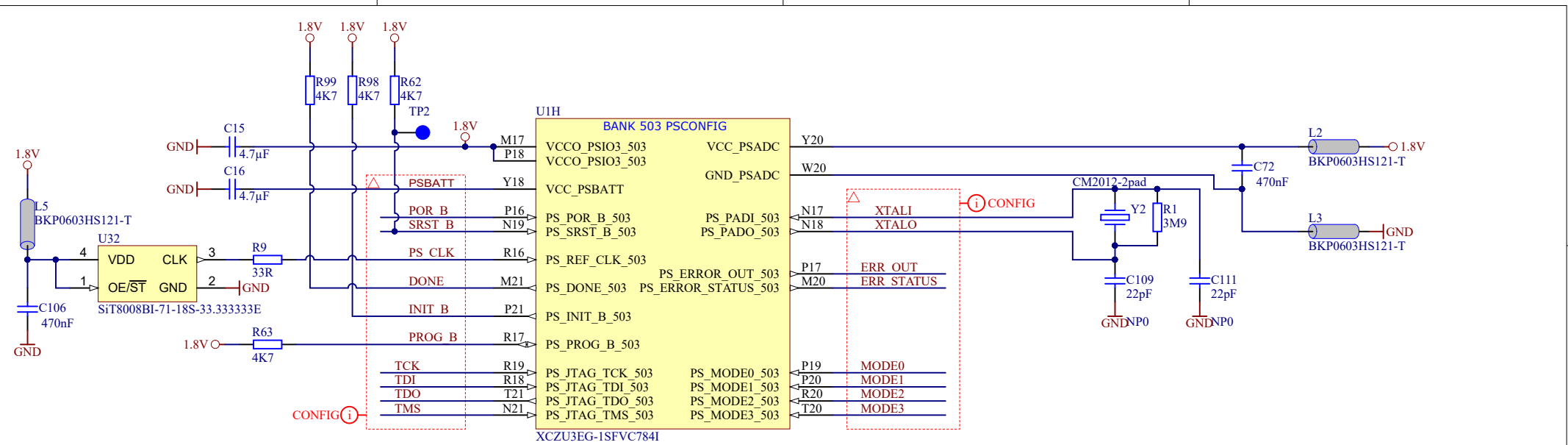
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	Title: TE0823 - Config		
	A4	Number: TE0823 [No Variations]	Rev. 01
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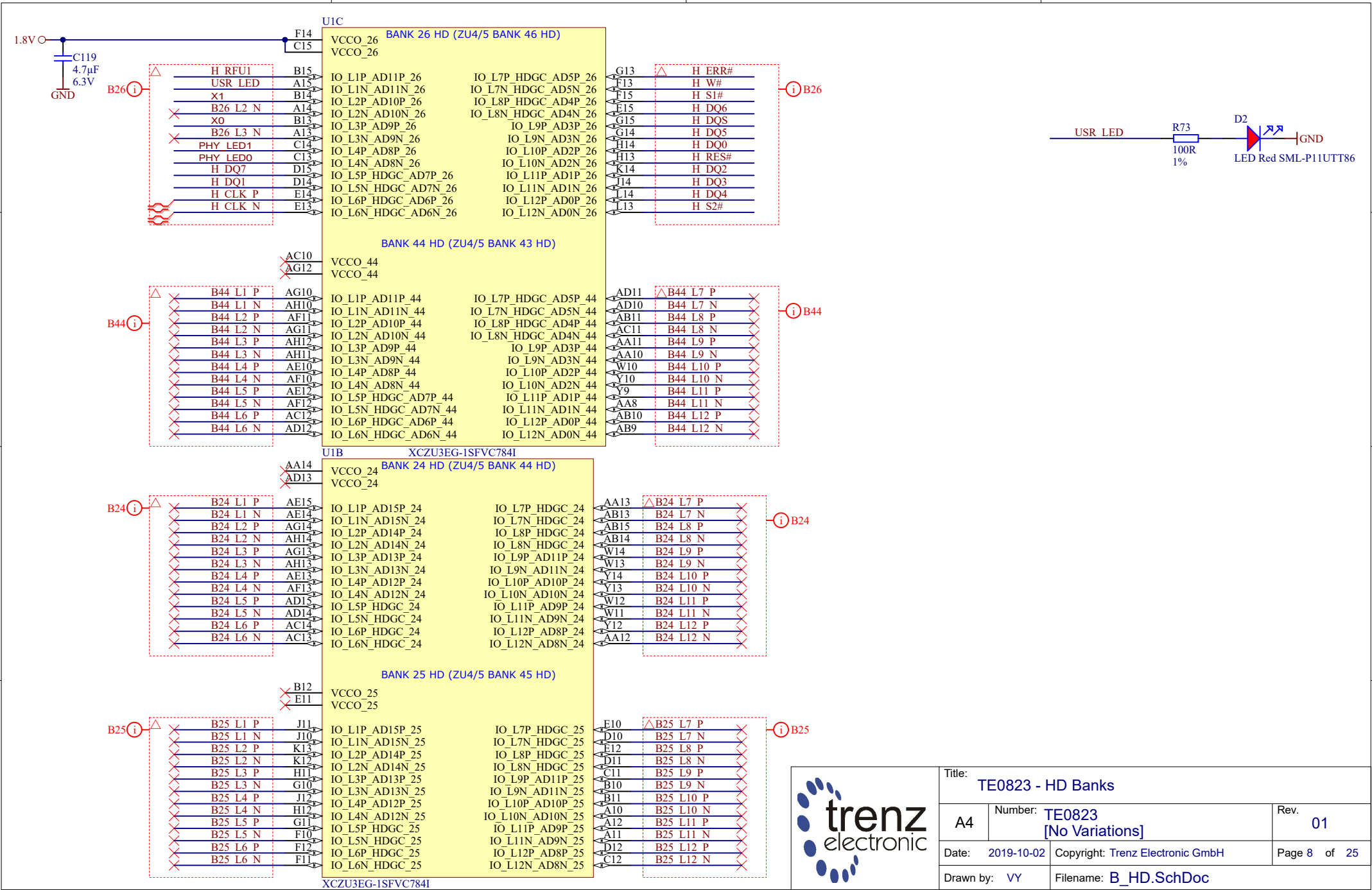
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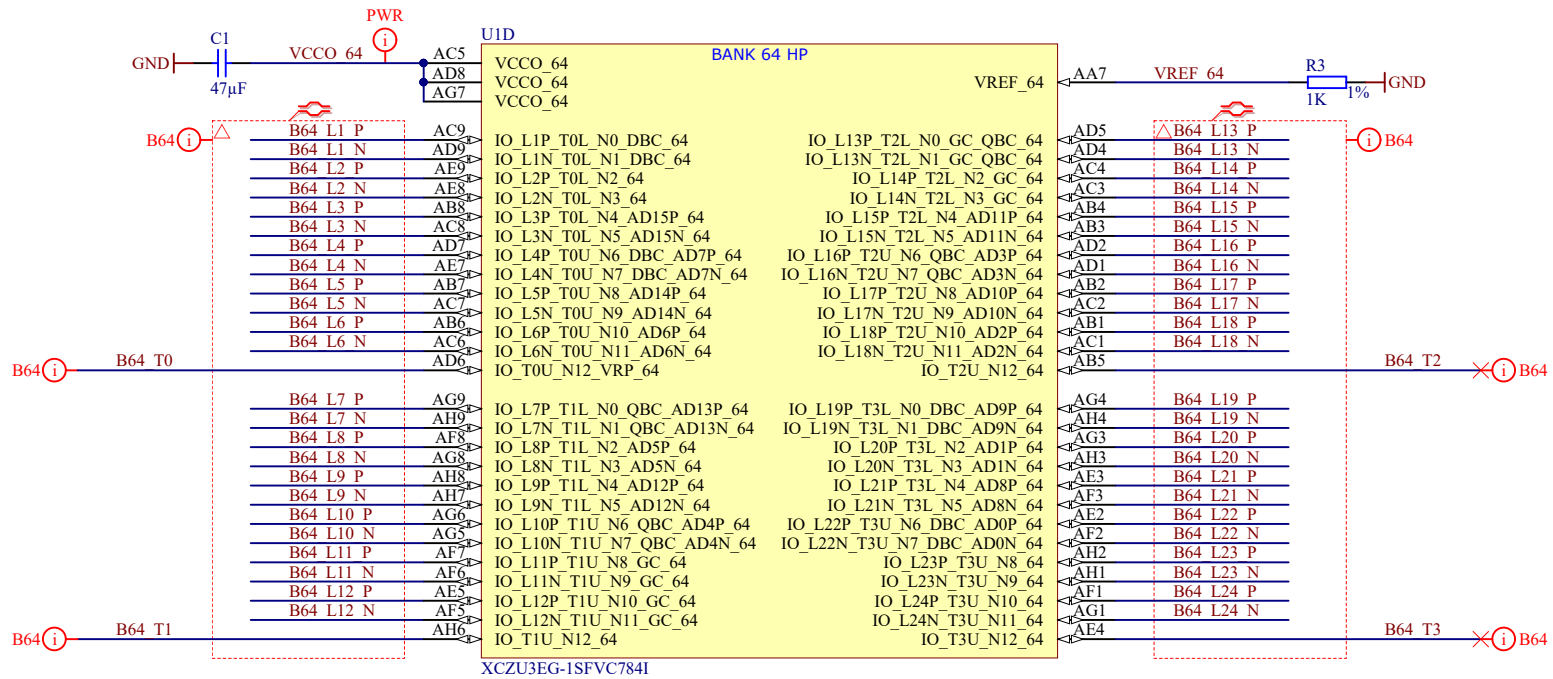
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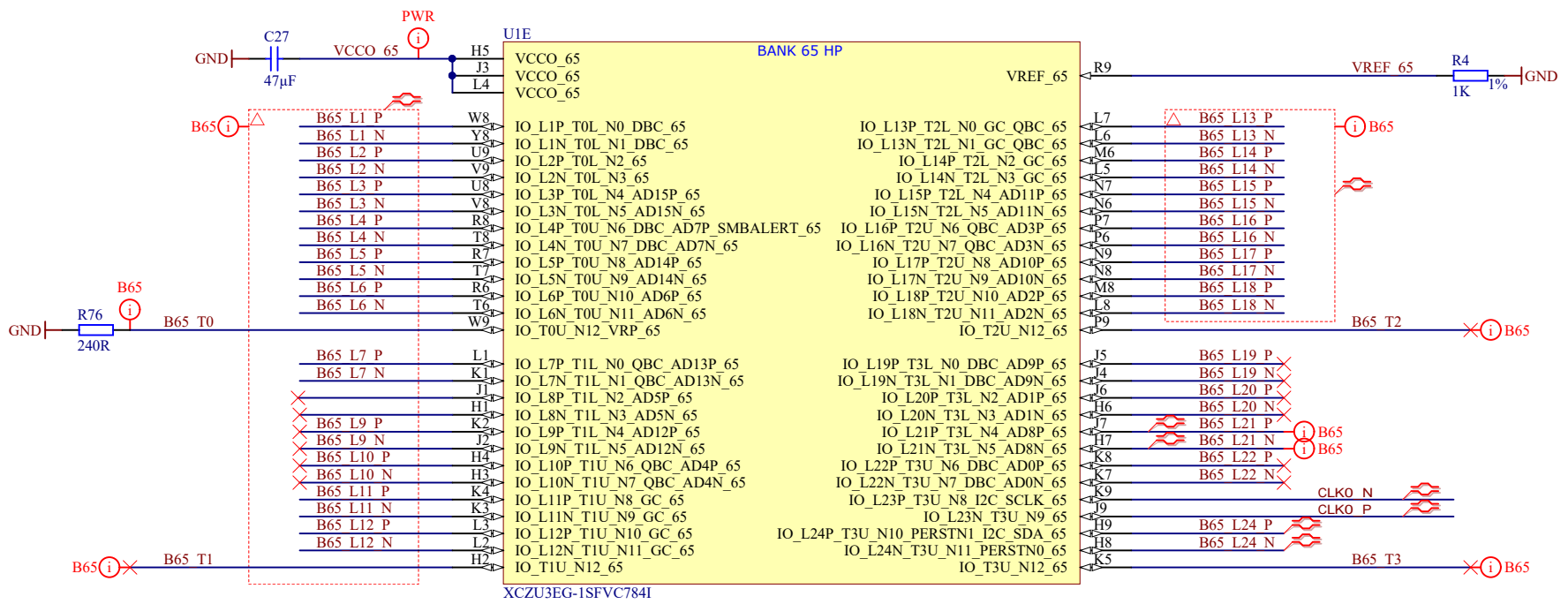
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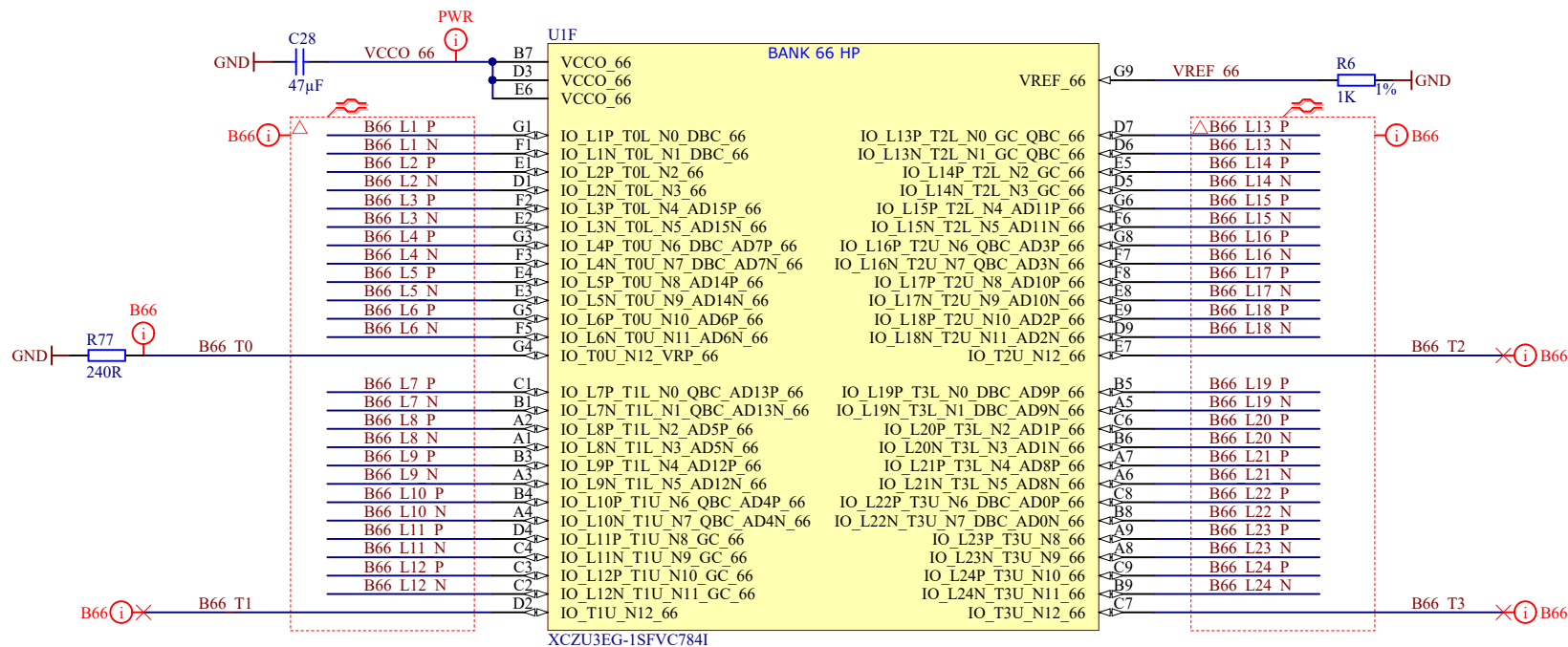

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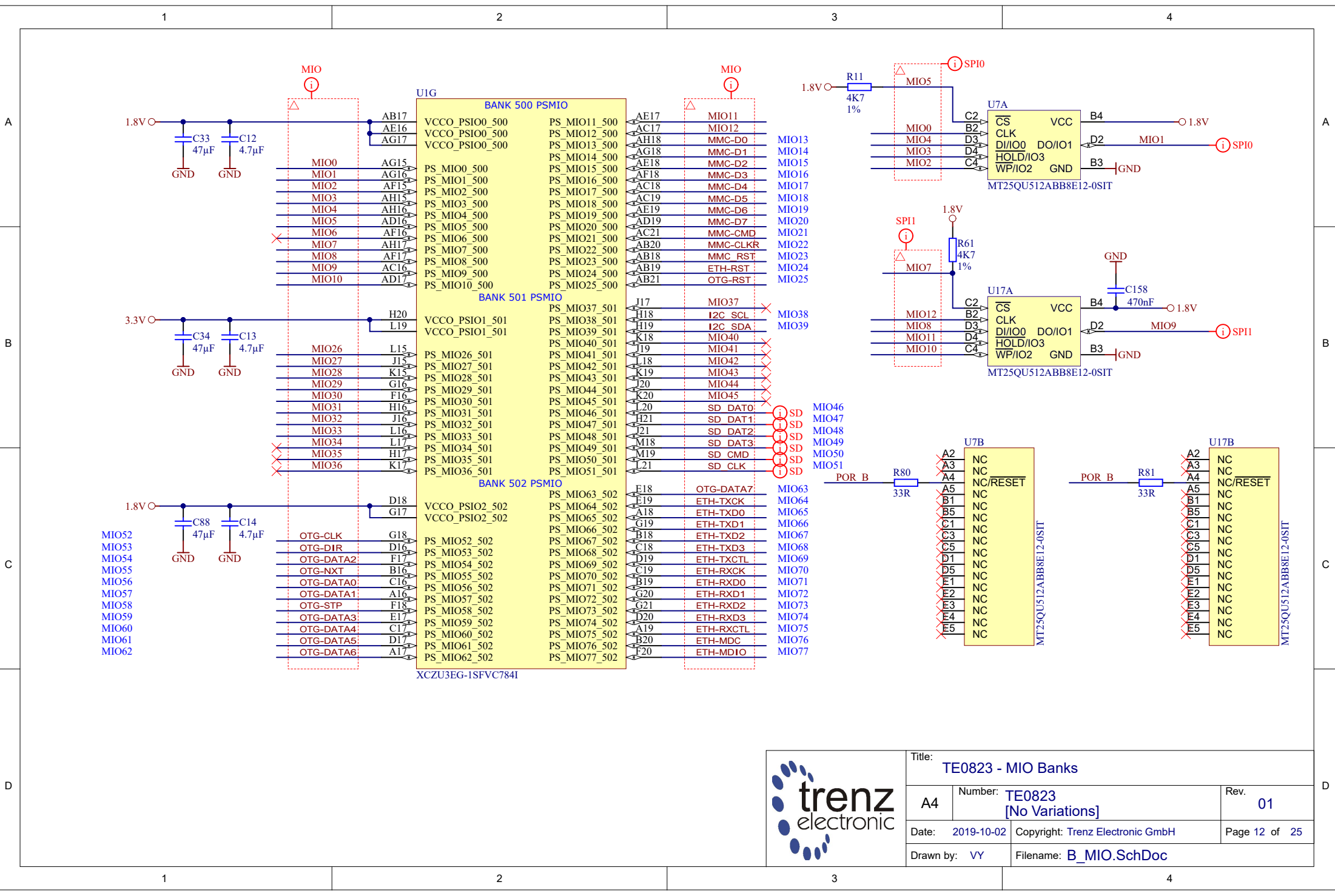
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Title: TE0823 - B66		
A4	Number: TE0823 [No Variations]	Rev. 01
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		Title: TE0823 - MIO Banks	
		A4	Number: TE0823 [No Variations]
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Drawn by: VY	Filename: B_MIO.SchDoc		

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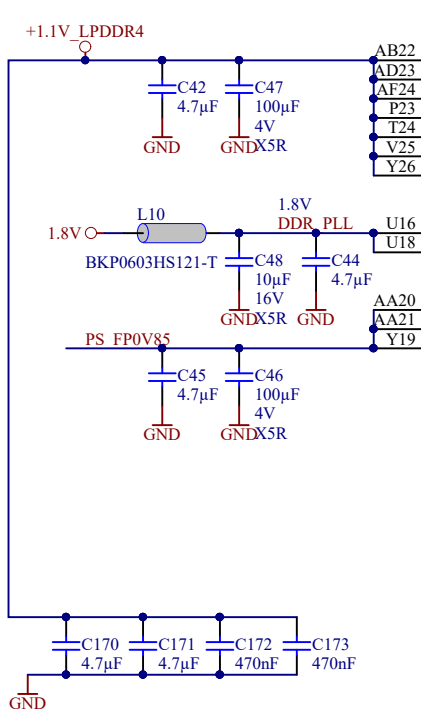
B

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U11

BANK 504 PSDDR

VCCO_PSDDR_504	PS_DDR_CK0_504	W25	LPDDR4_CKA_P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	LPDDR4_CKA_N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	LPDDR4_CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	LPDDR4_CKB_P
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	LPDDR4_CKB_N
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	LPDDR4_CKE1
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	LPDDR4_CAA0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	LPDDR4_CAA1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	LPDDR4_CAA2
VCC_PSDDR_PLL	PS_DDR_A3_504	AA28	LPDDR4_CAA3
VCC_PSDDR_PLL	PS_DDR_A4_504	Y27	LPDDR4_CAA4
VCC_PSDDR_PLL	PS_DDR_A5_504	AA27	LPDDR4_CAA5
VCC_PSINTFP_DDR	PS_DDR_A6_504	Y22	
VCC_PSINTFP_DDR	PS_DDR_A7_504	AA23	
VCC_PSINTFP_DDR	PS_DDR_A8_504	AA25	
VCC_PSINTFP_DDR	PS_DDR_A9_504	AB23	LPDDR4_CAB0
VCC_PSINTFP_DDR	PS_DDR_A10_504	AA26	LPDDR4_CAB1
VCC_PSINTFP_DDR	PS_DDR_A11_504	AB25	LPDDR4_CAB2
VCC_PSINTFP_DDR	PS_DDR_A12_504	AB26	LPDDR4_CAB3
VCC_PSINTFP_DDR	PS_DDR_A13_504	AB24	LPDDR4_CAB4
VCC_PSINTFP_DDR	PS_DDR_A14_504	AC24	LPDDR4_CAB5
VCC_PSINTFP_DDR	PS_DDR_A15_504	AC23	
VCC_PSINTFP_DDR	PS_DDR_A16_504	AC23	
VCC_PSINTFP_DDR	PS_DDR_A17_504	AC23	
PS_DDR_CS_N0_504		W27	LPDDR4_CS0_N
PS_DDR_CS_N1_504		V26	LPDDR4_CS1_N
PS_DDR_BA0_504		V23	
PS_DDR_BA1_504		W22	
PS_DDR_BG0_504		W24	ADDR_CTRL_B
PS_DDR_BG1_504		V22	
PS_DDR_PARITY_504		U23	
PS_DDR_RAM_RST_N_504		Y23	LPDDR4_RST
PS_DDR_ACT_N_504		U25	
PS_DDR_ALERT_N_504		U25	
PS_DDR_ZQ_504		U24	LPDDR4_ZQ
PS_DDR_ODT0_504		U28	
PS_DDR_ODT1_504		U26	

XCZU3EG-1SFVC784I

U1J

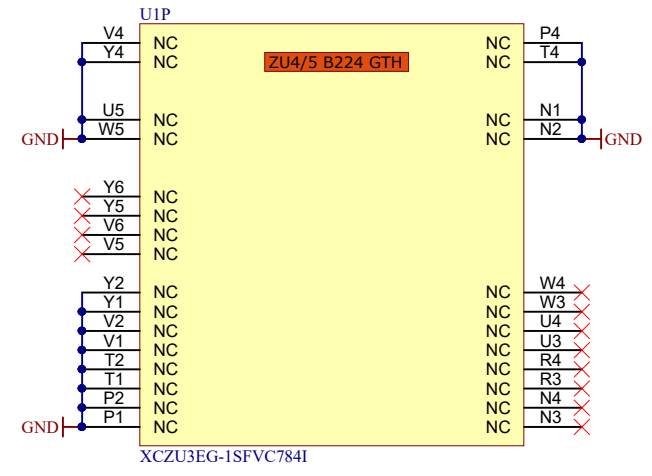
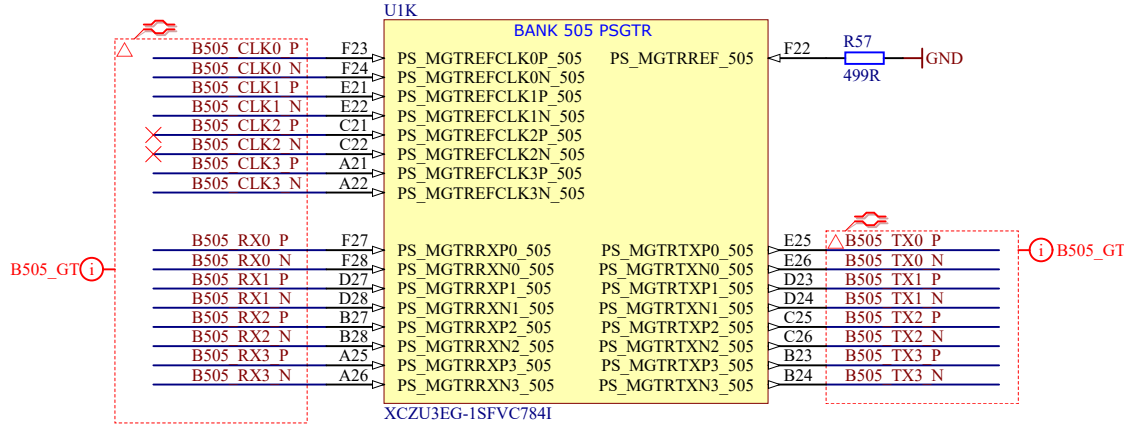
BANK 504 PSDDR

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LPDDR4_DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504	R22
LPDDR4_DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504	P22
LPDDR4_DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504	N22
LPDDR4_DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504	T23
LPDDR4_DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504	P24
LPDDR4_DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	R24
LPDDR4_DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	N24
LPDDR4_DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	H24
LPDDR4_DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504	J24
LPDDR4_DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504	M24
LPDDR4_DQ11	AD23	PS_DDR_DQ11_504	PS_DDR_DQ43_504	K24
LPDDR4_DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504	J22
LPDDR4_DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	H22
LPDDR4_DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504	K22
LPDDR4_DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504	J22
LPDDR4_DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504	M25
LPDDR4_DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504	M26
LPDDR4_DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504	L25
LPDDR4_DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504	L26
LPDDR4_DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504	K28
LPDDR4_DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504	L28
LPDDR4_DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504	M28
LPDDR4_DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504	N28
LPDDR4_DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504	L28
LPDDR4_DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504	K27
LPDDR4_DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504	H28
LPDDR4_DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504	H27
LPDDR4_DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504	G26
LPDDR4_DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504	G25
LPDDR4_DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504	K25
LPDDR4_DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504	J25
PS_DDR_DQS_P0_504	AF21	PS_DDR_DQ64_504	PS_DDR_DQ65_504	T28
PS_DDR_DQS_N0_504	AG21	PS_DDR_DQ66_504	PS_DDR_DQ67_504	R28
PS_DDR_DQS_P1_504	AF23	PS_DDR_DQ68_504	PS_DDR_DQ69_504	P27
PS_DDR_DQS_N1_504	AG23	PS_DDR_DQ70_504	PS_DDR_DQ71_504	P26
PS_DDR_DQS_P2_504	AF25	PS_DDR_DQ72_504		R25
PS_DDR_DQS_N2_504	AG25	PS_DDR_DQ73_504		P25
PS_DDR_DQS_P3_504	AE27	PS_DDR_DQ74_504		T25
PS_DDR_DQS_N3_504	AG27	PS_DDR_DQ75_504		R25
PS_DDR_DQS_P4_504	N23	PS_DDR_DQ76_504		P28
PS_DDR_DQS_N4_504	M23	PS_DDR_DQ77_504		P27
PS_DDR_DQS_P5_504	L23	PS_DDR_DQ78_504		P26
PS_DDR_DQS_N5_504	K23	PS_DDR_DQ79_504		R25
PS_DDR_DQS_P6_504	N26	PS_DDR_DQ80_504		P25
PS_DDR_DQS_N6_504	N27	PS_DDR_DQ81_504		T25
PS_DDR_DQS_P7_504	J26	PS_DDR_DQ82_504		R23
PS_DDR_DQS_N7_504	J27	PS_DDR_DQ83_504		H23
PS_DDR_DQS_P8_504	R27	PS_DDR_DQ84_504		L27
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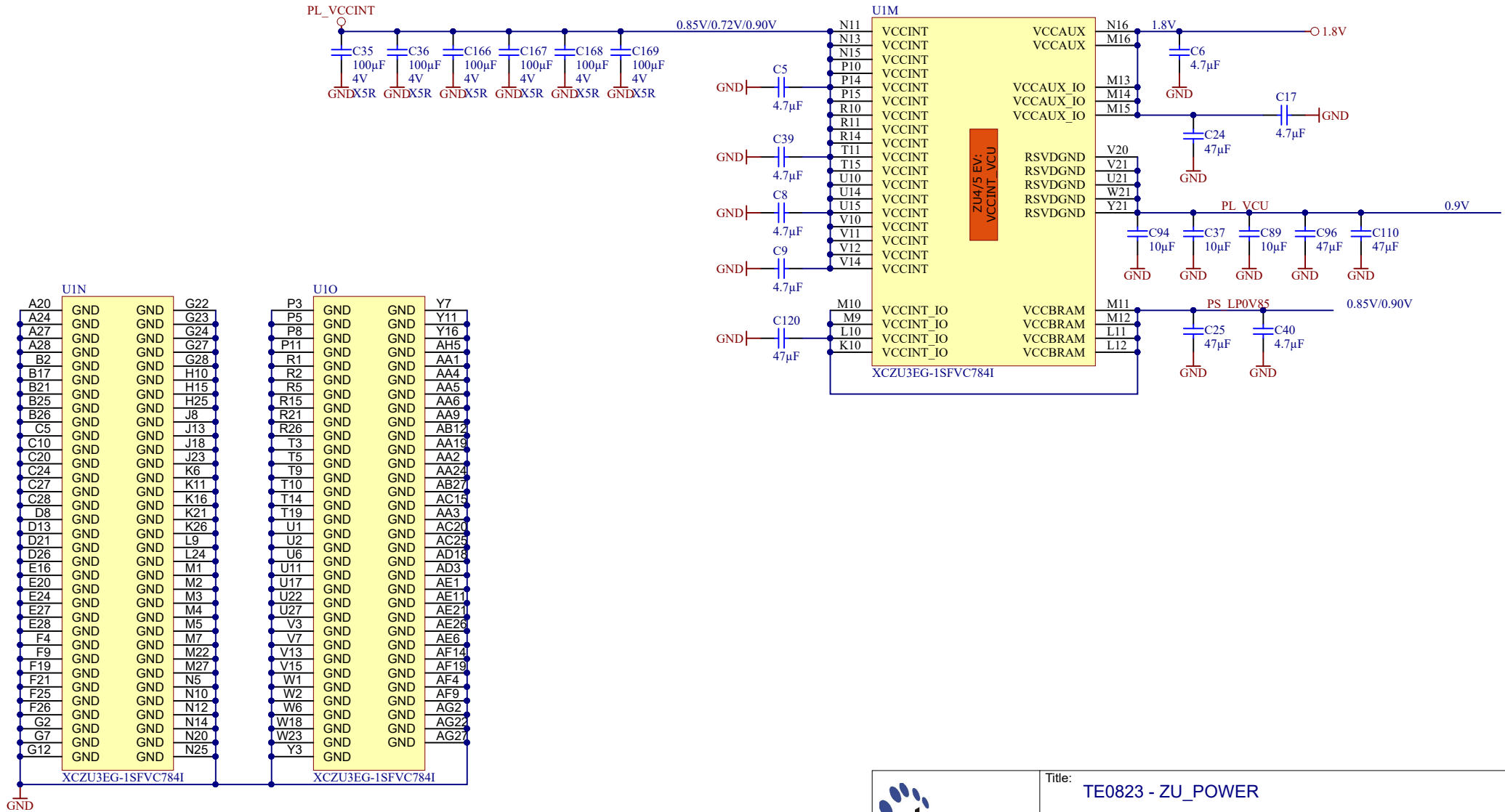
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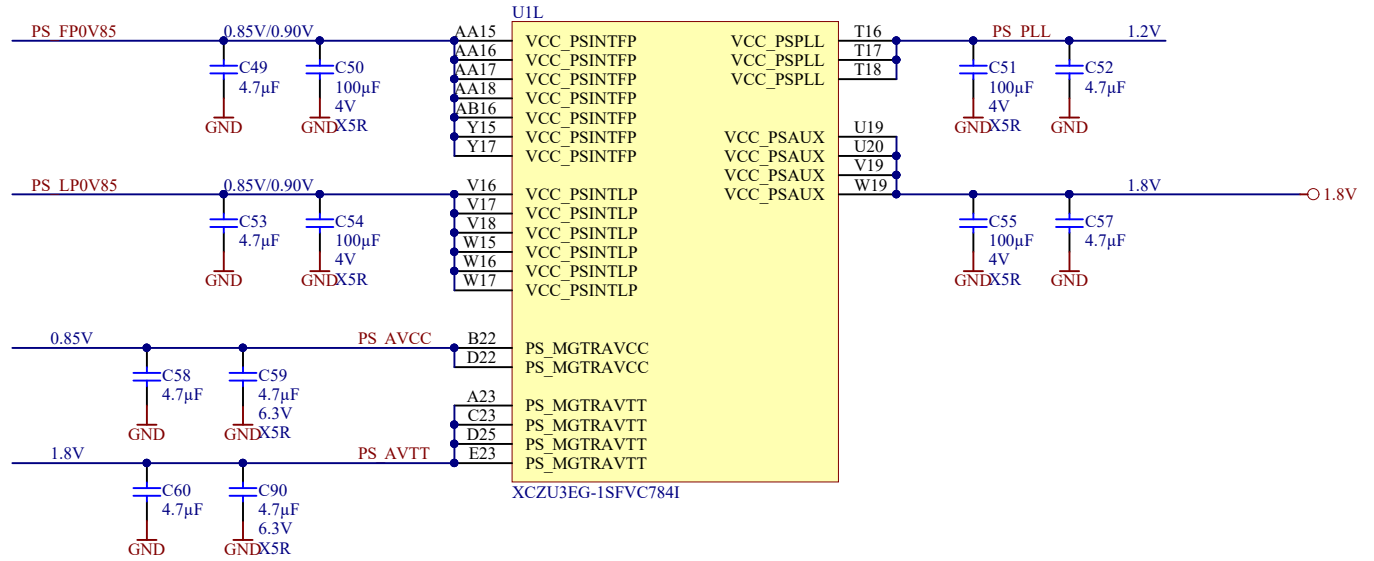
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Date: 2019-10-02	Copyright: Trenz Electronic GmbH	Page 13 of 25
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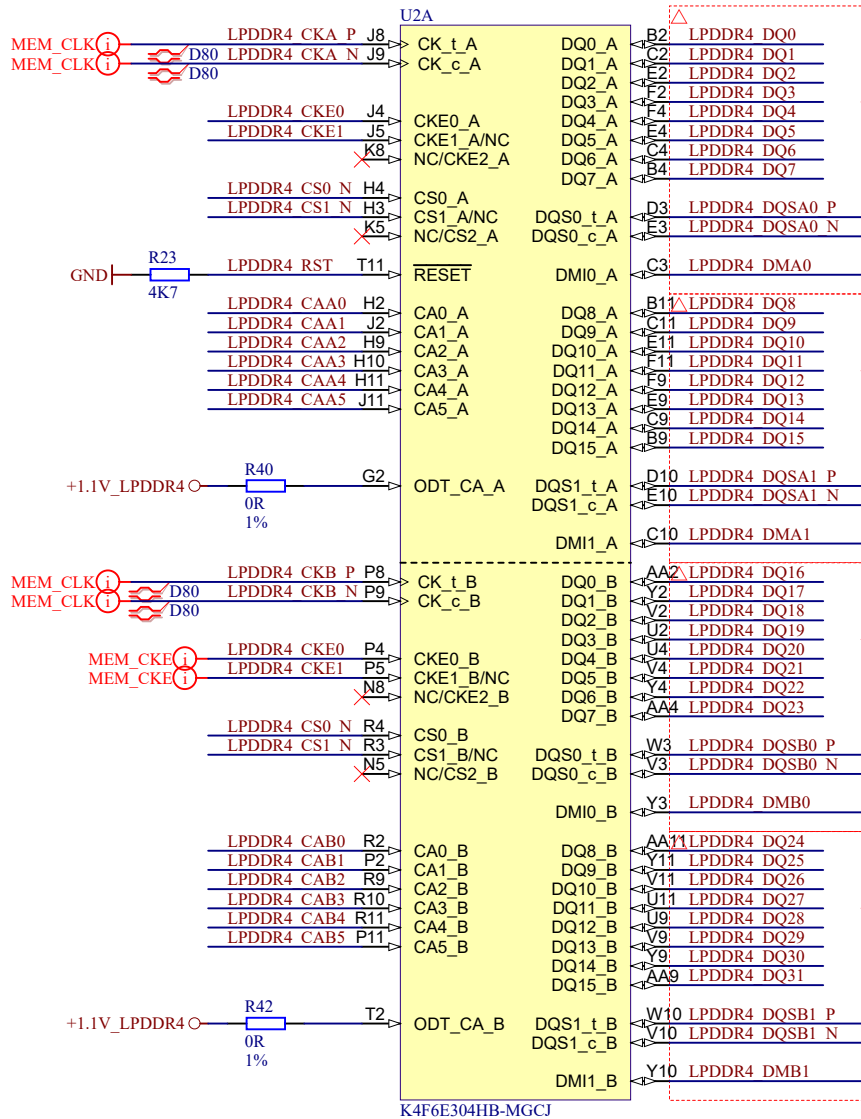
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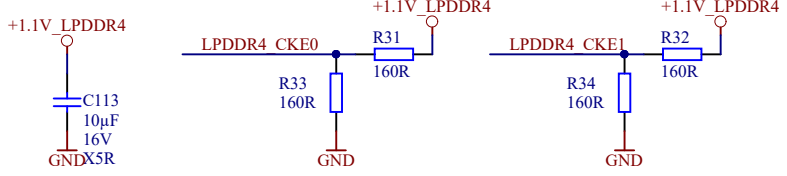
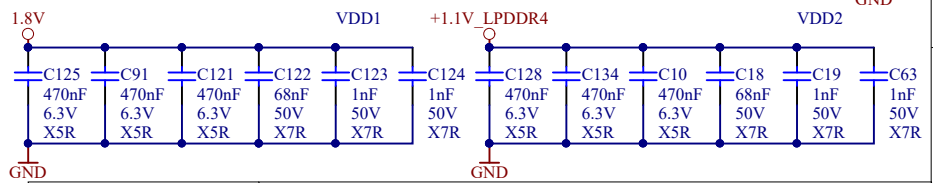
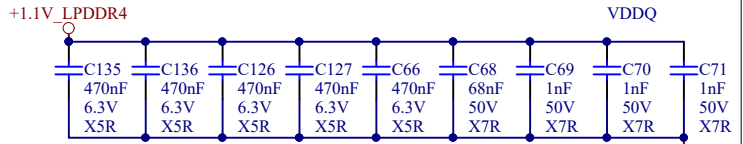
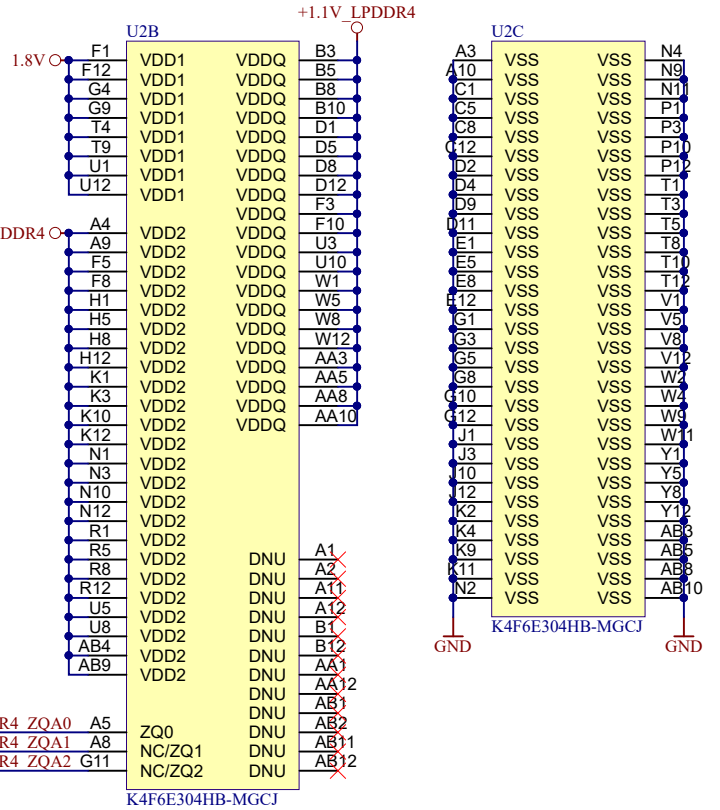


MEM_DQ_L0

MEM_DQ_L1

MEM_DQ_L2

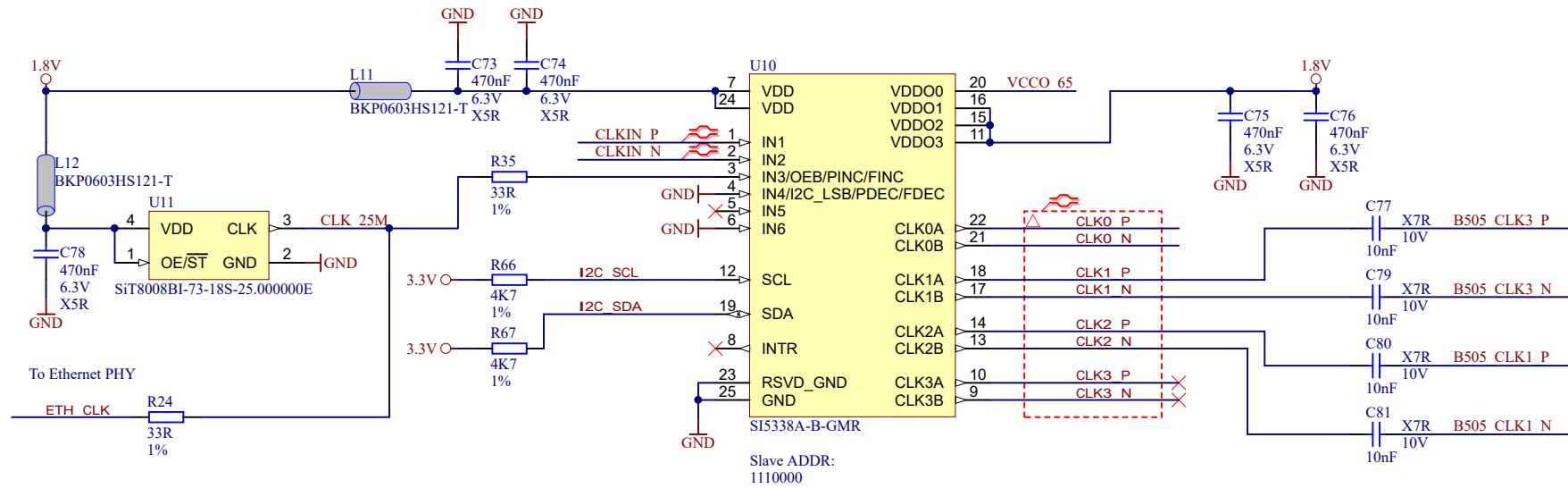
MEM_DQ_L3




trenz electronic

Title: **TE0823 - LPDDR4**

A4	Number: TE0823 [No Variations]	Rev. 01
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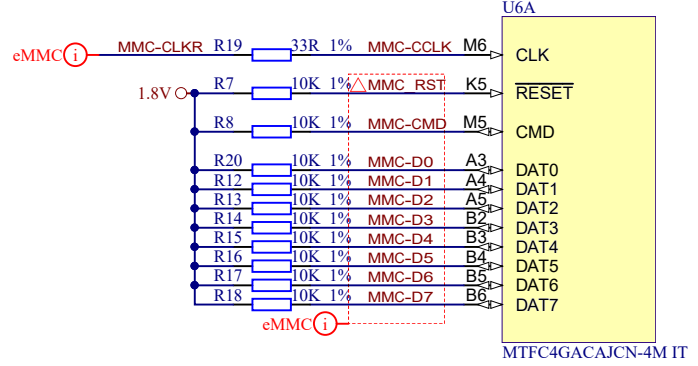


	Title: TE0823 - CLK		
	A4	Number: TE0823 [No Variations]	Rev. 01
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U6D

A1	NC	NC	H2
A2	NC	NC	H3
A8	NC	NC	H12
A9	NC	NC	H13
A10	NC	NC	H14
A11	NC	NC	J1
A12	NC	NC	J2
A13	NC	NC	J3
A14	NC	NC	J12
B1	NC	NC	J13
B7	NC	NC	J14
B8	NC	NC	K1
B9	NC	NC	K2
B10	NC	NC	K3
B11	NC	NC	K12
B12	NC	NC	K13
B13	NC	NC	K14
B14	NC	NC	L1
C1	NC	NC	L2
C3	NC	NC	L3
C7	NC	NC	L12
C8	NC	NC	L13
C9	NC	NC	L14
C10	NC	NC	M4
C11	NC	NC	M2
C12	NC	NC	M3
C13	NC	NC	M7
C14	NC	NC	M8
D1	NC	NC	M9
D2	NC	NC	M10
D3	NC	NC	M11
D4	NC	NC	M12
D12	NC	NC	M13
D13	NC	NC	M14
D14	NC	NC	N1
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E13	NC	NC	N9
E14	NC	NC	N10
F1	NC	NC	N11
F2	NC	NC	N12
F3	NC	NC	N13
F12	NC	NC	N14
F13	NC	NC	P1
F14	NC	NC	P2
G1	NC	NC	P8
G2	NC	NC	P9
G12	NC	NC	P11
G13	NC	NC	P12
G14	NC	NC	P13
H1	NC	NC	P14

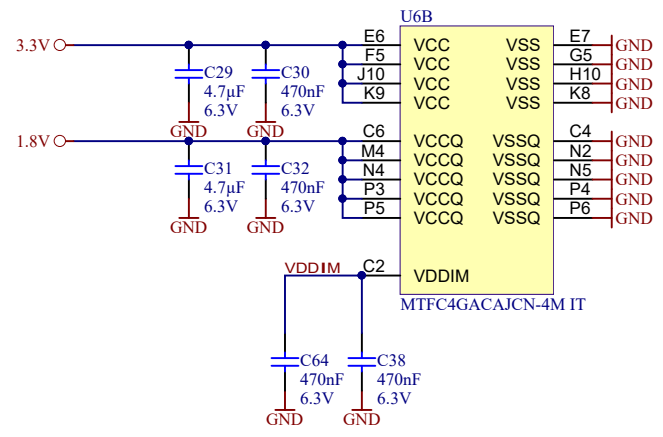
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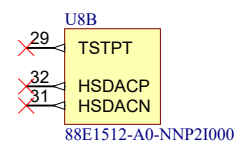
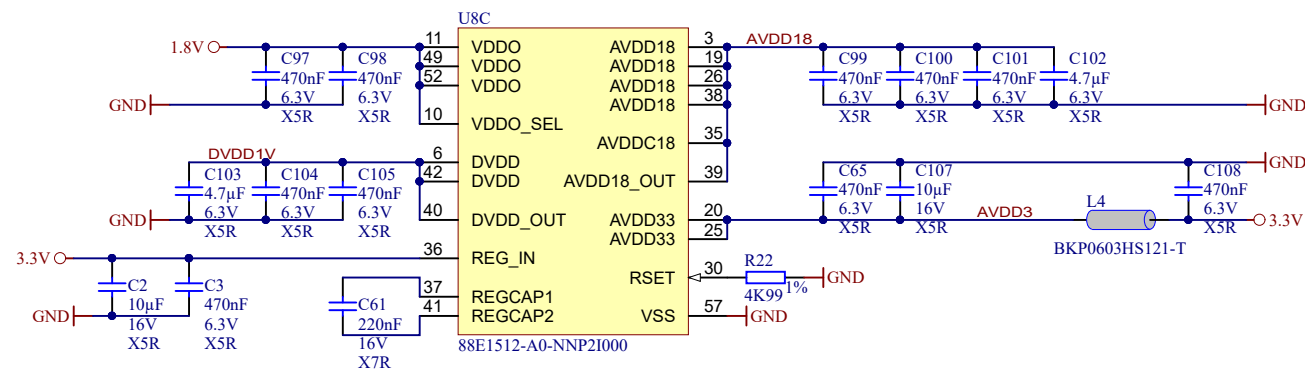
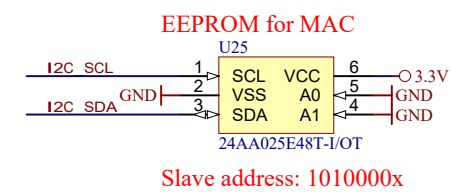
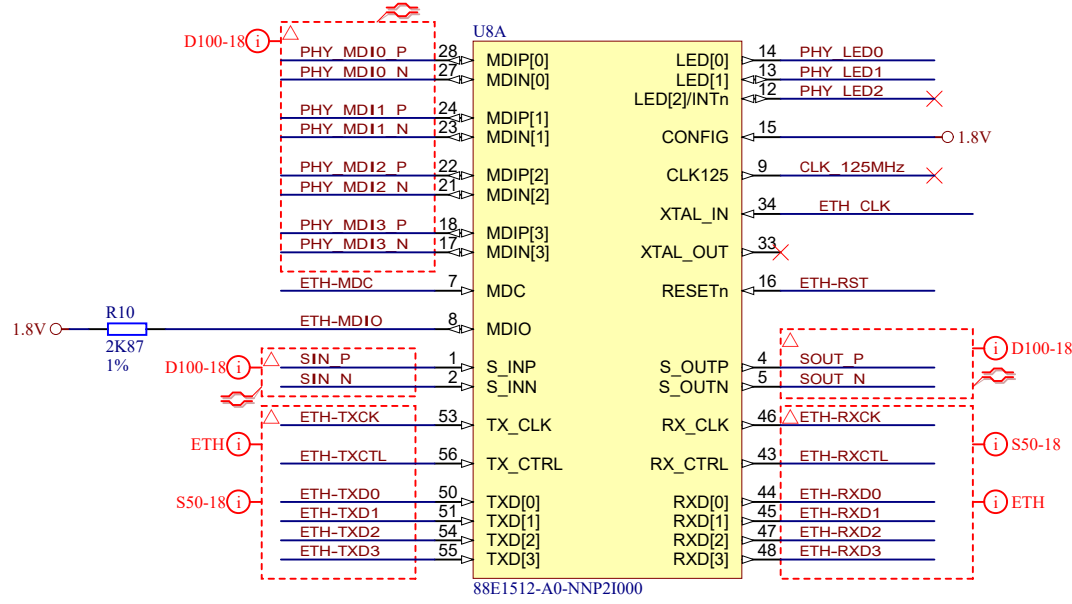
U6C

A6	RFU/VSS
A7	RFU
C5	RFU/NC
E5	RFU
E8	RFU
E9	RFU
E10	RFU
F10	RFU
G3	RFU/NC
G10	RFU
H5	RFU/DS
J5	RFU/VSS
K6	RFU
K7	RFU
K10	RFU
P7	RFU/NC
P10	RFU

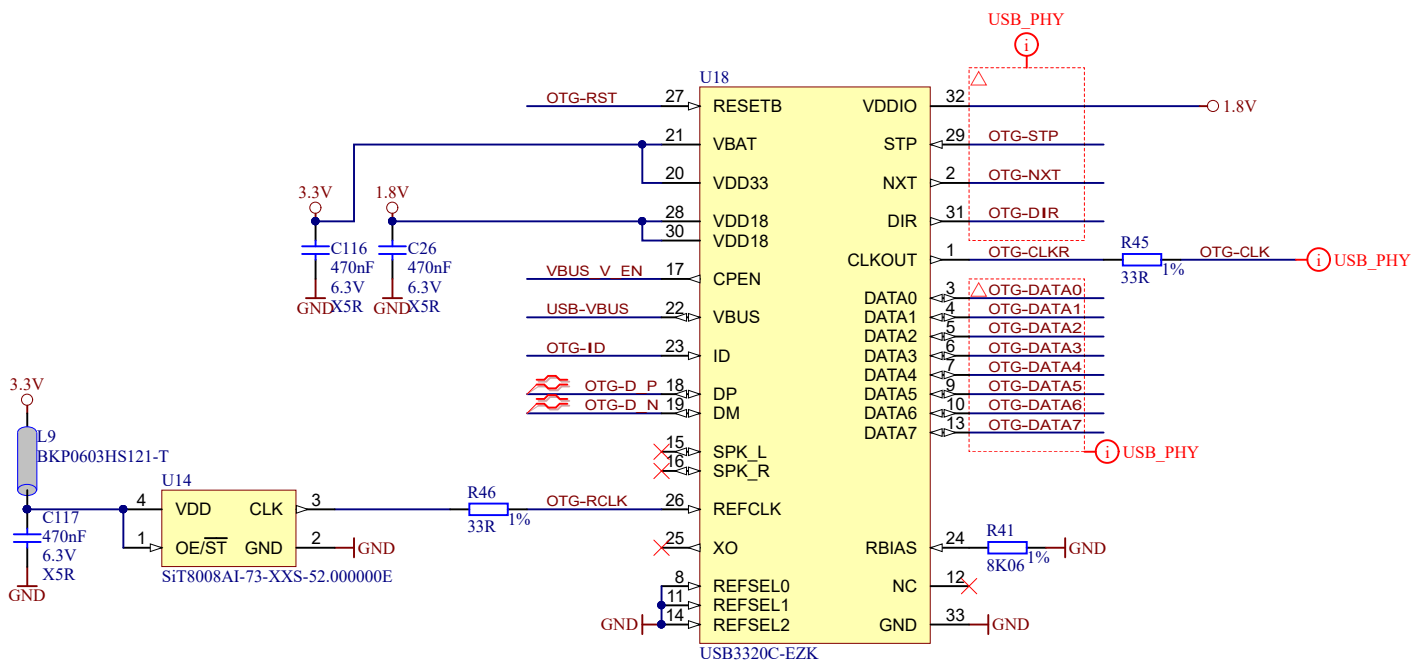
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Title: TE0823 - eMMC		
A4	Number: TE0823 [No Variations]	Rev. 01
Date: 2019-10-02	Copyright: Trenz Electronic GmbH	Page 19 of 25
Drawn by: VY	Filename: eMMC.SchDoc	



Title: TE0823 - Ethernet PHY		
A4	Number: TE0823 [No Variations]	Rev. 01
Date: 2019-10-02	Copyright: Trenz Electronic GmbH	Page 20 of 25
Drawn by: VY	Filename: ETH-PHY.SchDoc	



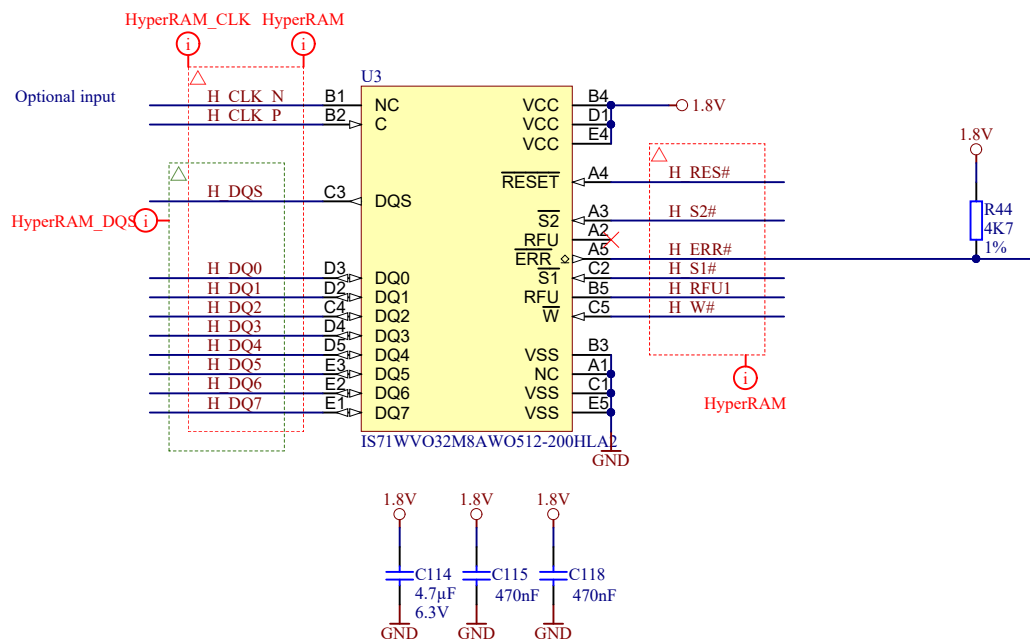
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			A4	Number: TE0823 [No Variations]
Date: 2019-10-02		Copyright: Trenz Electronic GmbH		Page 21 of 25
Drawn by: VY		Filename: USB-PHY.SchDoc		

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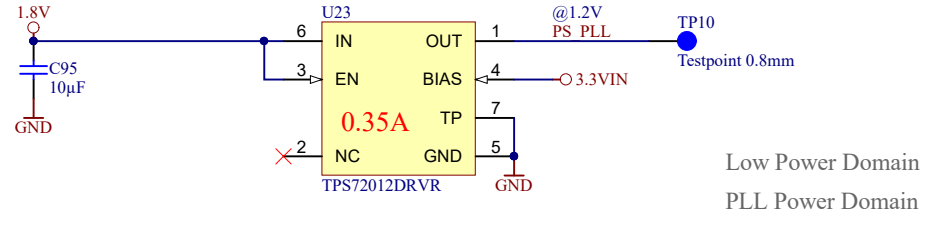
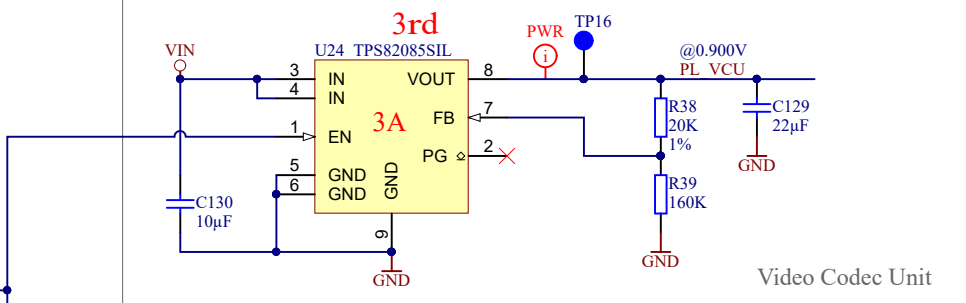
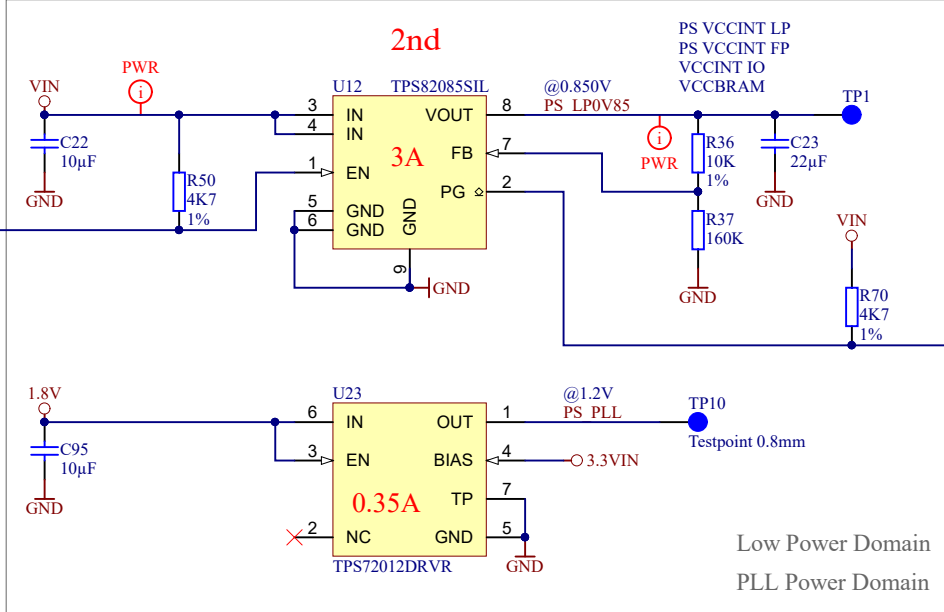
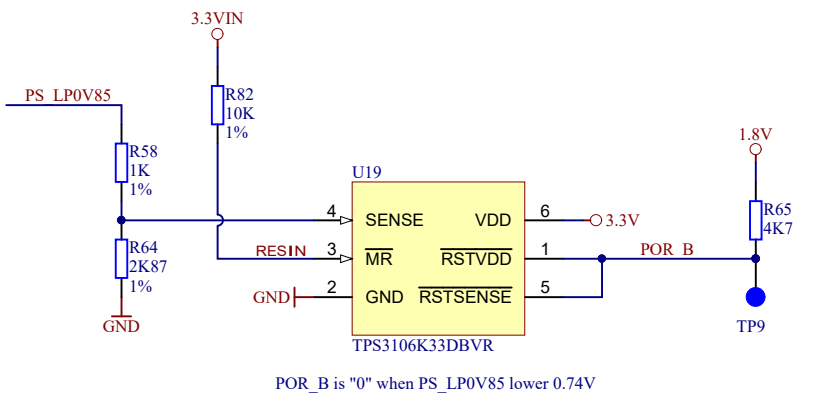
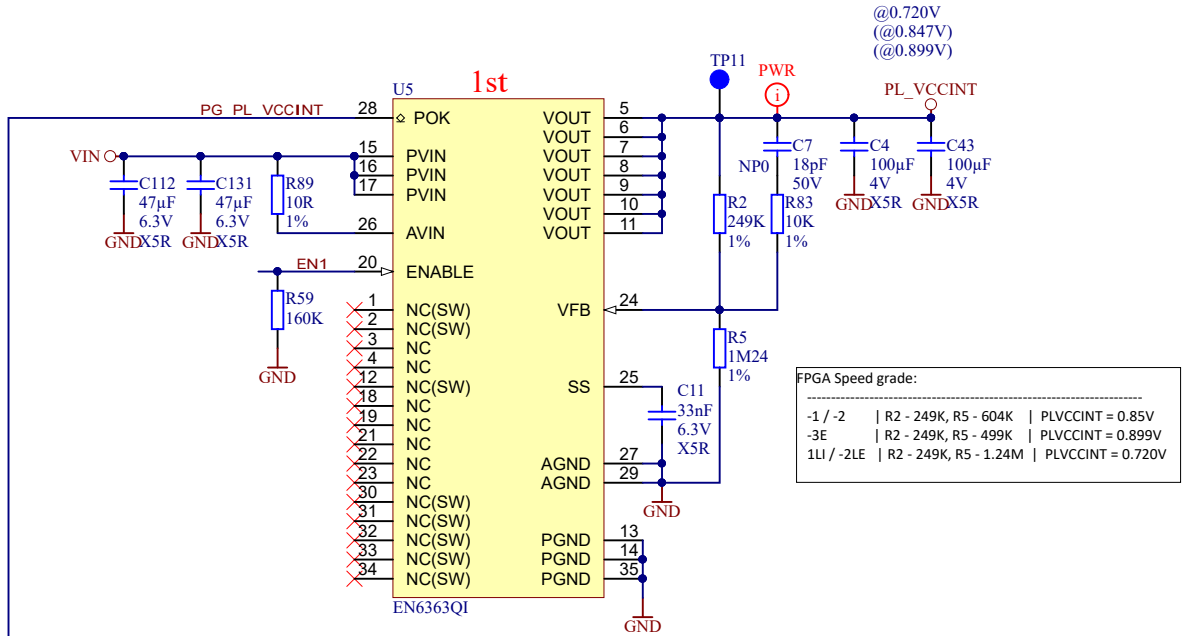
Title: TE0823 - HyperRAM/HyperFLASH		
A4	Number: TE0823 [No Variations]	Rev. 01
Date: 2019-10-02	Copyright: Trenz Electronic GmbH	Page 22 of 25
Drawn by: VY	Filename: HyperRAM.SchDoc	

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Title: TE0823 - POWER PL		
A4	Number: TE0823 [No Variations]	Rev. 01
Date: 2019-10-02	Copyright: Trenz Electronic GmbH	Page 23 of 25
Drawn by: VY	Filename: POWER.SchDoc	

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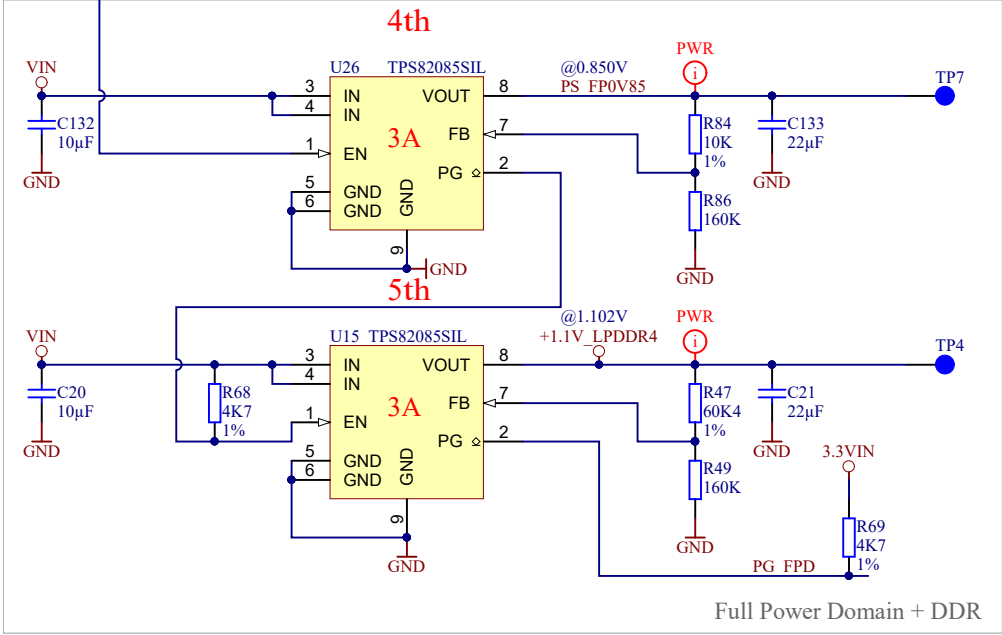
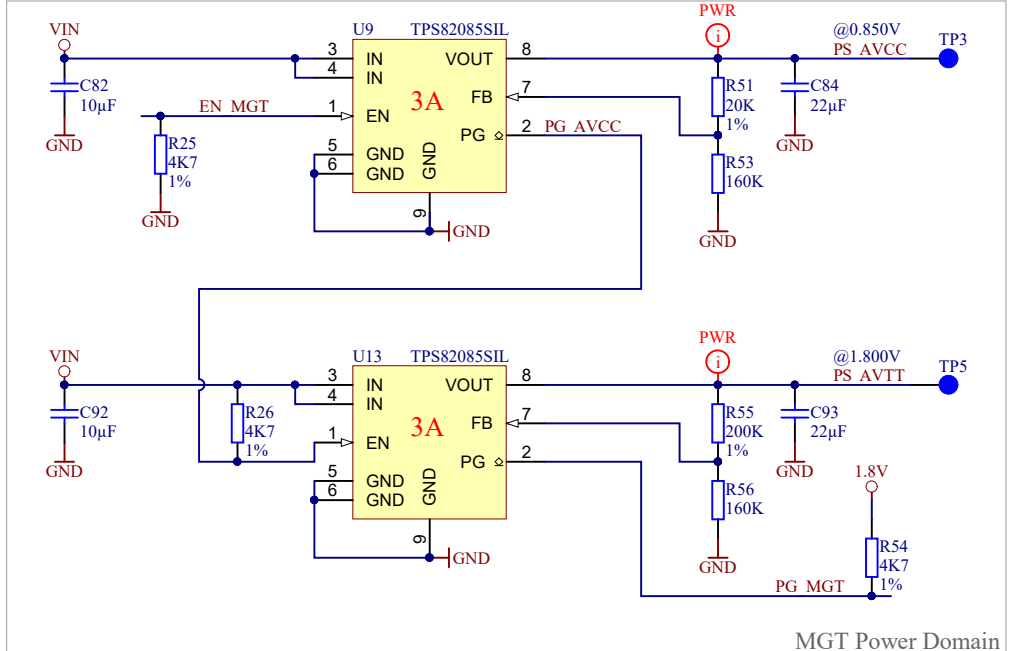
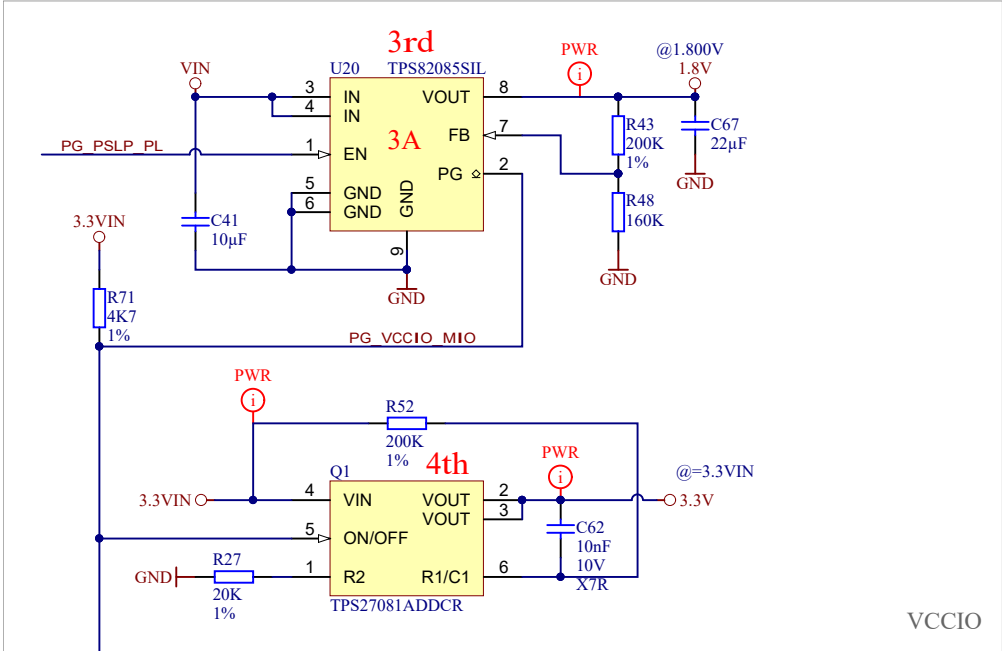
B

C

C

D

D



Title: TE0823 - POWER PS_DDR		
A4	Number: TE0823 [No Variations]	Rev. 01
Date: 2019-10-02	Copyright: Trenz Electronic GmbH	Page 24 of 25
Drawn by: VY	Filename: POWER_1.SchDoc	

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Revision 01a (01.07.2020):

- 1. VY: R38 value was changed to 20K (was: 40K2) to set VCU 0.9V

Revision 01b (29.10.2020):

- 1. VY: added block diagram
- 2. VY: added page "Legal notices"
- 3. VY: R51 value was changed to 10K (was: 20K) to set PS_VCU 0.85V

A

A

B


B

C

C

D

D

	Title: TE0823 - Revision Changes List		
	A4	Number: TE0823 [No Variations]	Rev. 01
	Date: 2019-10-02	Copyright: Trenz Electronic GmbH	Page 25 of 25
	Drawn by: VY	Filename: Revision Changes.SchDoc	

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